PAT-NO: JP405197352A

DOCUMENT-IDENTIFIER: JP 05197352 A

TITLE: LIQUID CRYSTAL DISPLAY SYSTEM

PUBN-DATE: August 6, 1993

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APPL-NO: JP04194354

APPL-DATE: July 22, 1992

INT-CL (IPC): G09G003/36, G02F001/133 , G02F001/133 , G09G003/20

ABSTRACT:

PURPOSE: To provide an LCD luminance control system capable of allowing an LCD to execute self-calibration and maximizing the number of gray scale levels.

CONSTITUTION: A TFTLCD display device 64 has a pel matrix, the respectively different drain voltage is impressed to the drain lines 68-1 to 68-j of different TFTs and the previously set number of gray scales is attained. Each different voltage is set up during the calibration of test pel and the test pel has substantially the same characteristics as a visible pel to be observed by a user. The characteristics of the test pel is measured at first and then a drain voltage value for attaining a different gray scale is mathematically extracted.

(19)日本国特許庁（JP）　(12) 公開特許公報 (A)　(11)特許出願公開番号 特開平5－197352
(43)公開日 平成5年(1993)8月6日

(51)Int.Cl.⁵	識別記号	庁内整理番号	F I	技術表示箇所
G09G 3/36		7319－5G		
G02F 1/133	550	7820－2K		
	575	7820－2K		
G09G 3/20	K	8621－5G		

審査請求 有　請求項の数12(全 8 頁)

(21)出願番号 特願平4－194354
(22)出願日 平成4年(1992)7月22日
(31)優先権主張番号 747217
(32)優先日 1991年8月19日
(33)優先権主張国 米国（US）

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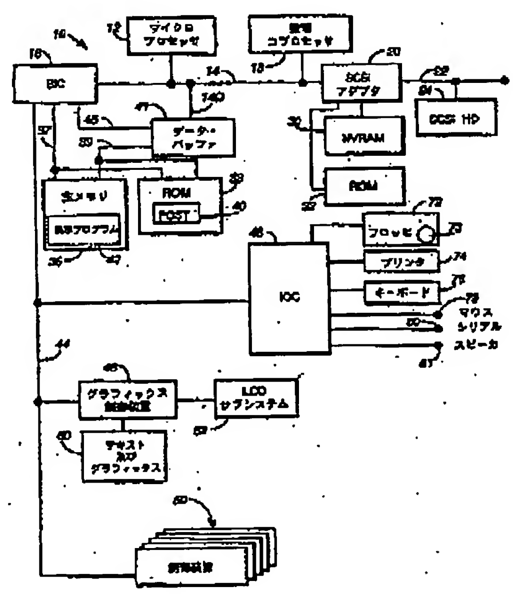
(54)【発明の名称】 液晶表示システム

(57)【要約】
【目的】 LCDの自己キャリブレーションを実施し、輝度或いはグレイ・スケール・レベルの数を最大化するLCD輝度制御システムを提供する。
【構成】 TFT LCD表示装置はペル・マトリクスを有し、異なるTFTのドレイン・ラインには異なるドレイン電圧が供給され、予め設定された数のグレイ・スケールを実現する。異なるドレイン電圧はテスト・ペルのキャリブレーション中にセットされ、このテスト・ペルはユーザにより見られる可視ペルと実質的に同一の特性を有する。テスト・ペルの特性が最初に測定され、異なるグレイ・スケールを実現するためのドレイン電圧値がこの測定から数理的に抽出される。



【特許請求の範囲】

【請求項1】薄膜トランジスタ（TFT）液晶表示（LCD）システムにおいて、
可視画素（ペル）マトリクスを含み、各ペルはTFTに結合される液晶材料を含み、前記液晶材料は前記TFTに供給されるドレイン電圧により制御される度合いの光を伝達し、
前記可視ペルと同一の特性を有するテスト・ペルと、
前記マトリスクに接続され、前記可視ペルにドレイン電圧を供給する複数の選択的にセット可能な可変電圧源と、
前記電圧源と前記ペルに接続され、各ペルにドレイン電圧を供給する電圧源を制御する制御手段と、
前記テスト・ペルと前記電圧源に接続されて、前記テスト・ペルの前記特性を測定し、異なるレベルのドレイン電圧を生成して、前記可視ペルに対し複数のレベルのグレイ・スケールを提供するように前記電圧源をセットするキャリブレーション手段とを含むことを特徴とするLCDシステム。

【請求項2】各電圧源は、
前記各電圧源により生成されるドレイン電圧の値を制御するデジタル値を記憶するレジスタと、
前記レジスタに接続され、前記レジスタに記憶される前記デジタル値をドレイン電圧のアナログ値に変換するデジタル－アナログ変換器とを含むことを特徴とする請求項1記載のLCDシステム。

【請求項3】前記キャリブレーション手段は、前記テスト・ペルの近傍に配置され、前記テスト・ペルを通じて伝送される光を測定し、前記光に比例する出力信号を生成するフォトダイオードを含むことを特徴とする請求項2記載のLCDシステム。

【請求項4】前記キャリブレーション・システムは更にデジタル・データ処理システム（DPS）を含み、該システムはプロセッサ、及び、該プロセッサに接続されてキャリブレーション・ルーチン及び測定結果を記憶するメモリを含み、
前記DPSは前記電圧源内の前記レジスタに接続され、前記レジスタに前記可変電圧源により生成される前記ドレイン電圧のレベルを制御する前記デジタル値を書き込むことを特徴とする請求項3記載のLCDシステム。

【請求項5】アナログ－デジタル変換器を含み、前記フォトダイオード及び前記DPSに接続されて、前記フォトダイオードからのアナログ出力をデジタル出力値に変換し、該出力値を前記メモリに記憶する手段を含むことを特徴とする請求項4記載のLCDシステム。

【請求項6】前記テスト・ペルはゲート・ライン及びドレイン・ラインを含み、前記キャリブレーション手段は、
前記ゲート・ラインに接続されるゲート・ドライバと、
前記ドレイン・ライン及び前記DPSに接続されるデジ

タルーアナログ変換器（DAC）とを含み、
前記DPSは一連の異なるデジタル・テスト信号を前記DACに転送し、それにより前記テスト・ペルを活動化して前記アナログ出力信号を生成し前記DPSは更に、前記メモリ内に記憶される前記デジタル出力値に関連して、前記デジタル・テスト信号を前記メモリに記憶することを特徴とする請求項5記載のLCDシステム。

【請求項7】前記DPSは前記デジタル・テスト信号と前記デジタル出力値を解析し、複数の異なるデジタル値を前記可変電圧源の前記レジスタに記憶することを特徴とする請求項6記載のLCDシステム。

【請求項8】前記異なるデジタル値は一連の増大するドレイン電圧レベルを生成し、各レベルと1つ前のレベルとの比は$\sqrt{2}$であることを特徴とする請求項7記載のLCDシステム。

【請求項9】前記異なるデジタル値は一連の増大するドレイン電圧レベルを生成し、各レベルと1つ前のレベルとの比は$e^{\ln CR/n}$であり、ここでeは自然対数の底、CRはコントラスト比、nはグレイ・スケール・レベル数であることを特徴とする請求項7記載のLCDシステム。

【請求項10】前記マトリクス内の前記可視ペルは行列に配列され、前記LCDシステムは複数のデマルチプレクサを含み、該デマルチプレクサの出力は前記可視ペルの駆動ラインに接続され、前記デマルチプレクサ入力は前記可変電圧源及びデータ信号源に接続され、前記データ信号の各々は任意のペルに対するグレイ・スケール値を含み、前記グレイ・スケール値は前記任意のペルに供給されるドレイン電圧レベルを決定することを特徴とする請求項1記載のLCDシステム。

【請求項11】前記データ信号源は前記データ信号を記憶するビデオ・ランダム・アクセス・メモリ（VRAM）を含むことを特徴とする請求項10記載のLCDシステム。

【請求項12】前記VRAMに接続されて前記データ信号を受信し、前記ペルに供給されるドレイン電圧信号を制御するタイミング手段を含み、ドレイン電圧レベルが各ペルに供給される度に、所定の固定時間、各ペルを繰り返しリフレッシュすることを特徴とする請求項11記載のLCDシステム。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明はデジタル的に動作する薄膜トランジスタ（TFT）液晶表示（LCD）システムの改善に関し、特に、自己キャリブレーションにより輝度或いはグレイ・スケール・レベルの数を最大化するLCDの輝度制御の改善に関する。

【0002】

【従来の技術】LCDは一般に、各々がTFTを含む画素或いはペル（PEL）により形成され、これらのTF

Tは供給される制御信号に応じ光を伝達する液晶材料に結合される。ペルの伝達率或いは見掛け上の輝度は液晶材料の極性の関数であり、これはドレイン電圧の大きさ及びゲート信号に伴いこうした電圧が供給される時間の関数である。制御信号が供給された後、TFTに付随する寄生容量が一時的にDC値を記憶するが、これは長時間周期において目的の伝達率を維持するために、リフレッシュ或いは再チャージされる必要がある。

【0003】LCDモニタ或いは表示装置に関し、ペルの完全なオンまたはオフの間に、伝達率に関する数多くの正確なステップを維持することは困難である。異なるレベル或いは値のドレイン電圧を供給することにより、任意のペルが異なる光量を伝達することが可能となり、ユーザには異なる輝度レベル或いは"グレイ・スケール"を有するように見受けられる。種々のグレイ・スケールを達成する従来の方法には、パルス幅変調（PWM）及びパルス振幅変調（PAM）がある。PWMでは固定のドレイン電圧がパルス幅により決定される異なる時間周期の間、供給される。PAMでは異なるドレイン電圧が同じ時間（固定パルス幅）供給される。PAMはハイエンドなTFT LCD モニタに好適である。PAMを使用することにより、ペルの平均極性はペルの光伝達率と共に変化し、グレイ調整が行われる。PAMではペルの伝達率は直接ペルのドレイン・ラインに供給される電圧のアナログ値により制御され、一方、ペルのゲート・ラインはデジタル的なゲート信号により活動化される。

【0004】現行のLCD製造プロセスでは、ペルのドレインに供給されるバイアス電圧に対し、完全に均一或いは予測可能な範囲のペルの伝達率を生じない。伝達率曲線の基本形状はよく知られているが、その絶対値は製造工程を経て生産される表示装置の間で大きく変化する。更に、人間の視覚が状況を複雑化する。なぜなら、人間の視覚はグレイ・スケールを1次のグラデーションに反し、対数的に捕らえるからである。これはグレイ・スケールの数が係数"n"で増加することにより、コントラスト比が $(\sqrt{2})^n$ で増加することが必要あることを意味し、ここでコントラスト比CRは最小伝達率に対する最大伝達率の比である。

【0005】任意の製造において、PAMに使用される異なるドレイン電圧値は、全ての表示装置に対して同一値にプリセットされるか、各表示装置は個々に工場キャリブレーションされる。前者の方法における問題は、異なる表示装置間での表示の大きな差であり、受諾可能なレベルに生産するために、グレイ・スケールのレベル数を制限しなければならない点である。後者の方法は表示装置のコストを増加させ、また、初期のセッティングに時間を取り過ぎないようにするなどのコンポーネントの寿命に対する配慮が施されていない。

【0006】

【発明が解決しようとする課題】本発明の目的は、組込み式自己キャリブレーション・システムを有する改善されたLCD TFT表示装置を提供する。

【0007】本発明の目的は、周期的に表示をキャリブレーションし、完全なオン－オフ間において、最大のグレイ・スケール・レベル数を実現するTFT LCD のための自己キャリブレーション・システムを提供する。

【0008】

【課題を解決するための手段】本発明によれば、TFT LCD 表示装置はペル・マトリクスを有し、ここでは異なるTFTのドレイン・ラインには異なるドレイン電圧が供給され、予め設定されたグレイ・スケール数を実現する。異なるドレイン電圧がキャリブレーション中に、テスト・ペルを通じてセットされる。これらのテスト・ペルは、実質的に、ユーザにより見られるペルと同じ特性を有する。テスト・ペルの特性が最初に測定され、異なるグレイ・スケールを実現するためのドレイン電圧の制御値が前記測定から抽出される。

【0009】

【実施例】図1を参照すると、本発明を実施するデータ処理システムの例を示し、このシステムはパーソナル・コンピュータ10を含み、これはPC DOS或いは OS／2などのオペレーティング・システムの下で動作し、アプリケーション・プログラムを実行する。コンピュータ10はマイクロプロセッサ12を含み、これはローカル・バス14に接続され、ローカル・バス14はバス・インタフェース制御装置（BIC）16、数理コプロセッサ18、及びSCSI（small computersystem interface） アダプタ20に接続される。マイクロプロセッサ12は好適には80386などの80xxxマイクロプロセッサ・ファミリの1つであり、またローカル・バス14はこうしたプロセッサのアーキテクチャに適合する従来のデータ、アドレス及び制御ラインを含む。アダプタ20はSCSIバス22にも接続され、このバスはC：driveとして指定されるSCSIハード・ドライブ（HD）24に接続される。SCSIバスはまた、他のSCSI装置（図示せず）にも接続可能である。アダプタ20は更にNVRAM30及び読出し専用メモリ（ROM）32にも接続される。

【0010】BIC16は2つの主な機能を実行し、1つは主メモリ36及びROM38をアクセスするためのメモリ制御装置の機能である。主メモリはダイナミック・ランダム・アクセス・メモリ（RAM）であり、これは複数のシングル・イン・ライン・メモリ・モジュール（SIMM）により構成され、マイクロプロセッサ12及び数理コプロセッサ18により実行されるプログラム及びデータを記憶する。メモリ36はデータを表示サブシステムに送信するための表示プログラム42を記憶し、これについては後述される。ROM38はPOSTプログラムを記憶する。POSTプログラム40はコン

ピュータ１０がパワー・オン或いはキーボード・リセットにより再スタートされる時に、１次テストすなわちシステムのＰＯＳＴを実行する。アドレス及び制御バス３７はＢＩＣ１６をメモリ３６及びＲＯＭ３８に接続する。データ・バス３９はメモリ３６及びＲＯＭ４８をデータ・バッファ４１に接続し、データ・バッファ４１は更にバス１４のデータ・バス１４Ｄに接続される。制御ライン４５はＢＩＣ１６とデータ・バッファ４１とを相互接続する。

【００１１】ＢＩＣ１６の他の主機能はマイクロチャネル（ＭＣ）・アーキテクチャによるバス１４と入出力バス４４間のインタフェースである。バス４４は更に入出力制御装置（ＩＯＣ）４６、グラフィックス制御装置４８、及び複数のＭＣコネクタ或いはスロット５０に接続される。制御装置４８は更にビデオＲＡＭ（ＶＲＡＭ）６０及びＬＣＤサブシステム６２に接続される。

【００１２】ＩＯＣ４６は複数の入出力装置のオペレーションを制御し、これらにはＡ：ｄｒｉｖｅとして指定されるフロッピ・ディスク・ドライブ７２、プリンタ７４、及びキーボード７６が含まれる。ドライブ７２は制御装置（図示せず）及び取り出し可能なフロッピ・ディスク或いはディスケット７３を含む。ＩＯＣ４６は、また、マウス・コネクタ７８、シリアル・ポート・コネクタ８０、及びスピーカ・コネクタ８１にも接続され、これらは種々のオプション装置をシステムに接続する。

【００１３】図２を参照すると、ＬＣＤサブシステム６２は"ｊ"列ｘ"ｋ"行のマトリクスにより構成されるペルを有するＴＦＴ ＬＣＤ６４ を含む。典型的なマトリクスは６４０列ｘ４８０行で構成される。複数のゲート・ライン６６－１からゲート・ライン６６－ｋはそれぞれの行内の全てのペルのゲートに接続されて、ペルの行に対してゲート信号を供給する。複数のドレイン・ライン６８－１からドレイン・ライン６８－ｊは異なる列のそれぞれのペルのドレイン・ラインに接続され、ペルの列に対してドレイン電圧信号を供給する。ゲート・ライン６６は行ドライバ６９により駆動され、ドレイン・ライン６８は列ドライバ７０により駆動される。個々のペルはゲート信号とドレイン電圧信号が同時に供給されることにより、或いはゲート・ライン及びドレイン・ライン６８上のレベルがそれぞれ個々のペルに接続されることにより活動化される。

【００１４】行ドライバ６９は従来通りＣＬＫ信号及び水平走査（ＨＳＣＡＮ）信号により動作され、後者の信号はタイミング及び制御回路８２から供給される。ＣＬＫ信号は水平同期（ＨＳＹＮＣ）信号及び垂直同期（ＶＳＹＮＣ）信号と共に、回路８２に供給される。後者の２つの信号は列タイミング及び制御回路８４に対しても、ＣＬＫ信号及びデータ信号と共に供給される。このデータ信号は制御装置４８及びＶＲＡＭ６０から供給され、各信号には個々のペル上に表示されるグレイ・スケール・レベルを表すデジタル値が含まれる。回路８２及び回路８４は同期して動作し、繰り返し且つ迅速にＬＣＤ６４に供給されるゲート信号及びドレイン信号を生成し、それによりユーザによって見られる目的のデータによる表示を生成する。

【００１５】列ドライバ７０は複数のラッチド・シフト・レジスタ８６を含み、これは垂直走査（ＶＳＣＡＮ）及びデータ信号を回路８４から受け取り、複数のライン８８－１からライン８８－ｊに各々"ｎ"ビットの一連のデジタル制御信号を出力する。"ｎ"の数は、表示技術的に実現可能であり目的とするグレイ・スケール・レベルの数（2^n） 或いは輝度レベルの数に基づき選択されるか、もしくは事前に決定される。ライン８８はそれぞれ複数のデマルチプレクサ（ＤＥＭＵＸ）９０－１からデマルチプレクサ（ＤＥＭＵＸ）９０－ｊに接続され、これらの出力はそれぞれドレイン・ライン６８に接続される。

【００１６】複数の2^n レベル・ラッチ（ＬＬ）９４はその出力がそれぞれ複数のデジタルーアナログ変換器（Ｄ／Ａ）９２の入力に接続される。ＬＬ９４は後述されるようにキャリブレーションの間にロードされ、デジタル制御信号は2^n 段階の異なるレベルのドレイン電圧を定義する輝度値を表す。これらの制御値はＤ／Ａ変換器９２により2^n 段階の異なるレベルのアナログ・ドレイン電圧に変換され、これらの電圧はＤＥＭＵＸ９０に伝達される。各ＤＥＭＵＸは９２の出力に現れる電圧レベルの１個をドレイン・ライン６８上に駆動し、それにより活動化ゲート信号を受け取る列内の１つのペルを駆動し、こうしてＤＥＭＵＸに供給されるデータ信号値に依存する輝度レベルが表現される。ＬＬ９４にはキャリブレーション処理の間にキャリブレーション・システム９６から伝達される値がロードされ、これについては後に詳述される。

【００１７】ＬＣＤ６４は前述のペル・マトリクスを囲む不透明マスク１００を有し、テスト・ペル９８はユーザからは見ることのできないマスクの背後に配置される。テスト・ペルはキャリブレーション・システム９６に接続され、図３に示されるフォトダイオード１０２を動作させる。図３を参照すると、テスト・ペル９８は可視ペルと同時に形成され、これと同一の特性を有し、表示装置のキャリブレーションのための信頼性のあるテストを提供する。フォトダイオード１０２はペル９８が発光する光を受光するように配置され、こうした光の輝度を示す出力電圧を生成する。ペル９８はキャリブレーションの間に、ゲート信号をゲート・ドライバ１０４から、またドレイン信号をＤ／Ａ変換器１０６から受け取る。変換器１０６は変換器９２と同一の変換特性を有し、そのアナログ出力値は任意のデジタル入力値に対して同一である。ゲート・ドライバ１０４はフリー・ランニング発振器であり、可視ペルの周波数及びデューティ

・サイクルに一致する。キャリブレーションの間に、テスト・ペルは可視ペルの場合と同じリフレッシュ周波数により駆動され、テスト・ペルの特性と可視ペルのそれとの直接的な相関を提供する。ある表示装置が製造されると、個々のペルの特性には若干の相違が生じる可能性がある。単一のテスト・ペルの使用は受諾可能なテストの正確度を提供する必要があるが、本発明の範中には複数のテスト・ペルを使用し、これらの結果を平均することにより更に高い正確度を得ることも含まれる。

【0018】キャリブレーション・システム96はデジタル・データ処理システムを有し、これはマイクロプロセッサ108を含みマイクロプロセッサ108はバス118によりRAM110、ROM112、デコーダ126、及びデジタル－アナログ変換器（D／A）106に接続される。ROM112はキャリブレーション・プログラム或いはルーチンを114を記憶しこれはマイクロプロセッサ108において選択的に実行されてキャリブレーションを行う。キャリブレーションはLCDの最初のパワー・オン時に実行されるか、プロセッサ12（図1）がPOSTプログラム40を実行し、自己テスト制御を表示システムに渡す時点で実行される。表示技術に関して、温度、気圧などの変化が表示に影響を及ぼす場合には、キャリブレーションはこうした状態変化に応じて動的に行われてもよい。キャリブレーションの間に、フォトダイオード102のアナログ出力（DO）は増幅器122により増幅され、次にアナログ－デジタル変換器（A／D）124でデジタル化され、バス118上に転送されてテーブル116に記憶される。テーブル116は、また、それぞれのアナログ値DOを生成したデジタル・テスト値（DV）を記憶する。

【0019】キャリブレーション・システム96はテスト・モード及びトライステート・モードで動作する。テスト・モード中は、システム96はLL94に有効に接続されて、最初にキャリブレーション・テストを実行し、次にレベル・ラッチをロードする。その後、システム96はトライステート・モードにスイッチされて、LL94から切断され、LL94に記憶されるデジタル制御値はLCD64を動作させるための目的のグレイ・スケール・レベルを提供する。図4を参照すると、プロセッサ108によりキャリブレーション・ルーチン114が実行されると、ステップ130はフォトダイオード102の出力電圧を、テスト・ペル98に供給される一連のテスト・ドレイン電圧値の関数として測定する。こうした測定ではRAM110内にテーブル116を生成し、フォトダイオード出力DOに対応するテスト・ドレイン電圧DVの値を記憶する。テスト中に取得されるテスト値或いはサンプルの数は、任意の表示システムにおいて予め決定されるグレイ値のレベル数よりも大きい（例えば100倍）。これによりグレイの陰影強度が最適化される。

【0020】次にステップ134で、"n"段階のグレイ・スケール・レベルに対応するドレイン電圧を生成するために、LL94にロードするための異なる制御値が選択される。この選択はステップ136で決定され、ここではフォトダイオード出力に対するペル98へのテスト・ドレイン電圧入力の数理解析が行われる。こうした解析は好適には次に示す2つの公式または方程式の一方を使用して実施される。

【0021】

$$X(y+1)=X(y)\cdot\sqrt{2} \qquad (1)$$

【0022】ここで、X（y+1）は（y+1）番目のグレイ・スケール・レベルに対応するダイオード出力、X（y）は（y）番目のグレイ・スケール・レベルに対応するダイオード出力、X（1）はテスト中に検出される最小のダイオード出力、yは1から"n"の範囲の値、"n"はグレイ・スケール・レベル数である。

【0023】nは $n=\ln(CR)/((\ln 2)/2)$ で示され、ここで"CR"はコントラスト比であり、"ln"は標準自然対数であり、"n"は整数に切り捨てられる。

【0024】

$$X(y+1)=X(y)\cdot e^{\ln CR/n} \qquad (2)$$

【0025】ここで、eは自然対数の底であり、他の全ての項は既に定義済みである。

【0026】式1の使用により、グレイ・スケール・ステップ比が約1.4で生成され、これは人間が識別することのできる近接する輝度或いはグレイ・スケール・レベルに関する最小の比率と見なされる。式2では1.4より大きなステップ比が生成され、結果的に、表示はより輝度に関して不連続となり、近接するレベル間でコントラストの差が識別できるようになる。ダイオードのステップ・レベルが決定されると、テーブル116がアクセスされて、こうしたレベルを生成するDV値がルックアップされ、次にステップ138で選択されたデジタル値をデジタル制御値としてLL94に記憶する。これはデジタル制御値をバス118上に送信し、これがデコーダ126からライン128を介して送られるラッチ信号によりラッチされる。キャリブレーション完了後の通常のオペレーションにおいては、種々のレベルのドレイン・ライン電圧が固定幅パルスとしてPAMによりペルに繰り返し供給され、異なるグレイ・スケールを生成する。

【0027】前述の詳細なキャリブレーション処理はモノクロLCDに関して述べられてきたが、当業者にはレッド、グリーン及びブルー（RGB）の液晶に対しても同様にキャリブレーションを実施することにより、前述の処理をカラー化LCDについても適用できることが理解されよう。また、当業者には、本発明の範中を逸脱することなく、詳細における他の変更が可能であることも理解されよう。

【0028】

【発明の効果】以上説明したように、本発明によれば、表示を周期的にキャリブレーションし、完全なオンとオフのレベルの間に、最大数のグレイ・スケール・レベルを実現するTFT LCDの自己キャリブレーション・システムを提供できる。

【図面の簡単な説明】

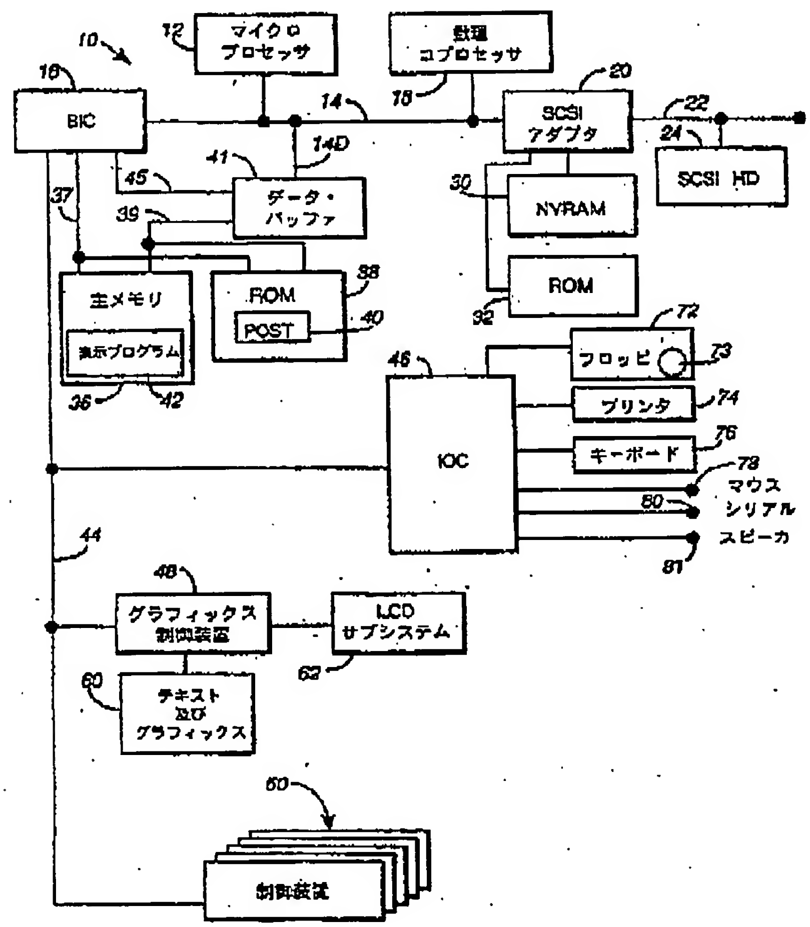
【図1】本発明を実施するデータ処理システムのブロック図である。

【図2】図1のLCDサブシステムのブロック図である。

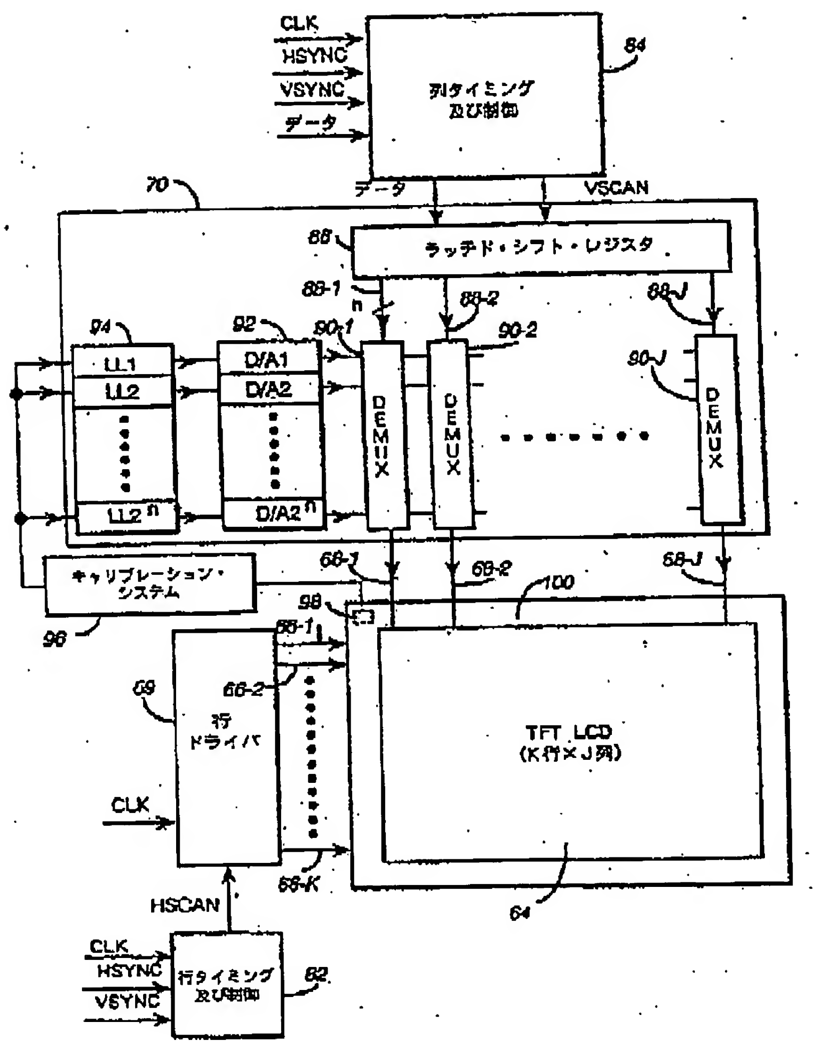
【図3】図2のLCDサブシステムのキャリブレーション・システムを主に示すブロック図である。

【図4】本発明で使用されるキャリブレーション処理の概要フロー図である。

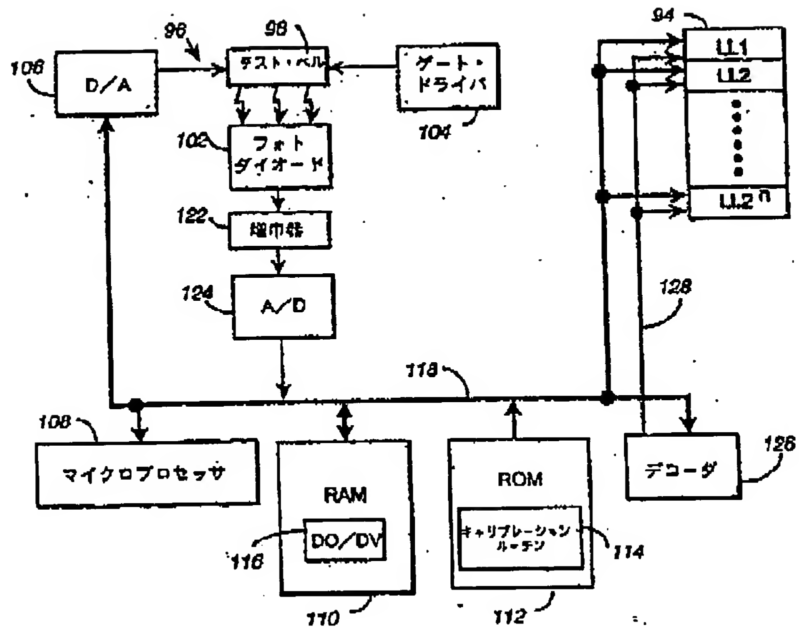
【図1】



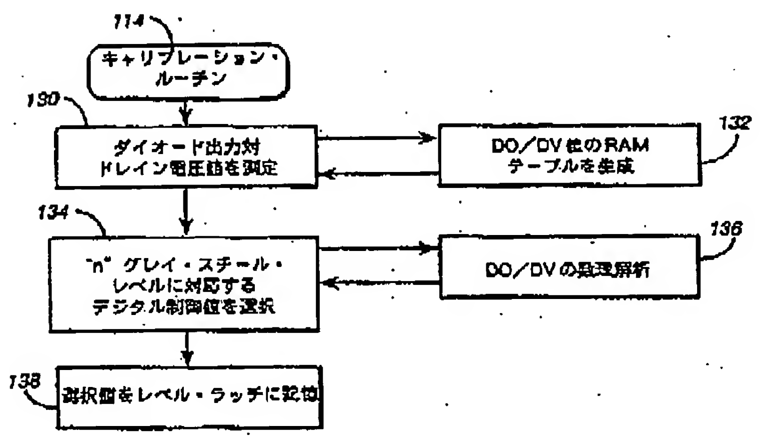
【図2】


CLK
HSYNC
VSYNC
データ
列タイミング
及び制御
84
70
データ
VSCAN
88
ラッチド・シフト・レジスタ
88-1
n
88-2
88-J
94
92
90-1
90-2
90-J
LL1
LL2
LL2^n
D/A1
D/A2
D/A2^n
DEMUX
DEMUX
DEMUX
キャリブレーション・
システム
96
68-1
68-2
68-J
100
98
66-1
66-2
69
行
ドライバ
CLK
TFT LCD
(K行×J列)
66-K
64
HSCAN
CLK
HSYNC
VSYNC
行タイミング
及び制御
62

【図3】


96
98
94
106
D/A
テスト・セル
ゲート・ドライバ
104
LL1
LL2
LL2 n
102
フォト ダイオード
122
増巾器
124
A/D
128
118
108
マイクロプロセッサ
RAM
ROM
デコーダ
126
DO/DV
キャリブレーション ルーチン
116
114
110
112

【図4】


114
キャリブレーション・ルーチン
130
ダイオード出力対ドレイン電圧値を測定
DO/DV 値のRAMテーブルを生成
132
134
"n" グレイ・スケール・レベルに対応するデジタル制御値を選択
DO/DVの数理解析
136
138
選択値をレベル・ラッチに記憶

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CLAIMS

[Claim(s)]
[Claim 1] In a thin film transistor (TFT) liquid crystal display (LCD) system Each pel contains the liquid crystal ingredient combined with TFT including a visible pixel (pel) matrix. The test pel which said liquid crystal ingredient transmits the light of the degree controlled by the drain electrical potential difference supplied to said TFT, and has the same property as said visible pel, Selectively [plurality] which is connected to said MATORISUKU and supplies a drain electrical potential difference to said visible pel The adjustable voltage source which can be set, The control means which controls the voltage source which is connected to said voltage source and said pel, and supplies a drain electrical potential difference to each pel, Connect with said test pel and said voltage source, measure said property of said test pel, and the drain electrical potential difference of different level is generated. The LCD system characterized by including a calibration means to set said voltage source so that the gray scale of two or more level may be offered to said visible pel.
[Claim 2] Each voltage source is a LCD system according to claim 1 characterized by including the register which memorizes the digital value which controls the value of the drain electrical potential difference generated by said each voltage source, and the digital-to-analog converter which changes into the analog value of a drain electrical potential difference said digital value which is connected to said register and memorized by said register.
[Claim 3] Said calibration means is a LCD system according to claim 2 characterized by including the photodiode which generates the output signal which is arranged near said test pel, measures the light transmitted through said test pel, and is proportional to said light.
[Claim 4] Said DPS is a LCD system according to claim 3 characterized by writing in said digital value which controls the level of said drain electrical potential difference which is connected to said register of said electrical-potential-difference Gennai, and is generated by said register according to said adjustable voltage source including the memory with which this system is further connected to a processor and this processor including digital data processing system (DPS), and said calibration system remembers a calibration routine and a measurement result to be.
[Claim 5] The LCD system according to claim 4 characterized by including a means to connect with said photodiode and said DPS, to change the analog output from said photodiode into a digital output value including an analog-digital converter, and to memorize this output value in said memory.
[Claim 6] Said test pel includes a gate line and a drain line. Said calibration means The gate driver connected to said gate line and the digital-to-analog converter (DAC) connected to said drain line and said DPS are included. Said DPS transmits the digital test signal from which a single string differs to said DAC. It is the LCD system according to claim 5 which carries out activation of said test pel by that cause, and is characterized by generating said analog output signal and said DPS memorizing said digital test signal in said memory in relation to said digital output value further memorized in said memory.
[Claim 7] Said DPS is a LCD system according to claim 6 characterized by memorizing the digital value from which said digital test signal and said digital output value are analyzed, and plurality differs to said

register of said adjustable voltage source.
[Claim 8] the drain voltage level to which, as for said different digital value, a single string increases -- generating -- the ratio of each level and the level in front of one -- root2 it is -- LCD system according to claim 7 characterized by things.
[Claim 9] the drain voltage level to which, as for said different digital value, a single string increases -- generating -- the ratio of each level and the level in front of one -- eln CR/n it is -- LCD system according to claim 7 by which e is characterized by a contrast ratio and n of the bottom of a natural logarithm and CR being the numbers of gray-scale level here.
[Claim 10] It is arranged by the matrix and, as for said visible pel within said matrix, said LCD system contains two or more demultiplexers. The output of this demultiplexer is connected to the actuation line of said visible pel. Said demultiplexer input is connected to said adjustable voltage source and the source of a data signal. For said gray-scale value, each of said data signal is a LCD system according to claim 1 characterized by determining the drain voltage level supplied to the pel of said arbitration including the gray-scale value over the pel of arbitration.
[Claim 11] Said source of a data signal is a LCD system according to claim 10 characterized by including the video random access memory (VRAM) which memorizes said data signal.
[Claim 12] The LCD system according to claim 11 characterized by repeating predetermined fixed time and each pel whenever a drain voltage level is supplied to each pel including a timing means to control the drain voltage signal which is connected to said VRAM, receives said data signal, and is supplied to said pel, and refreshing.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to an improvement of the intensity control of LCD which maximizes the number of brightness or gray-scale level by the self-calibration especially about the improvement of a thin film transistor (TFT) liquid crystal display (LCD) system which operates in digital one.
[0002]
[Description of the Prior Art] Generally LCD is formed of the pixel or pel (PEL) in which each contains TFT, and these TFT(s) are combined with the liquid crystal ingredient which transmits light according to the control signal supplied. The transmissibility or the apparent brightness of a pel is the polar function of a liquid crystal ingredient, and this is a function of time amount with which such an electrical potential difference is supplied in connection with the magnitude and the gate signal of a drain electrical potential difference. although the parasitic capacitance which accompanies TFT memorizes DC value temporarily after a control signal is supplied, in order that this may maintain the target transmissibility in a long duration period -- refresh -- or it needs to be re-charged.
[0003] It is difficult to maintain many exact steps about transmissibility about a LCD monitor or a display, perfect ON of a pel, or while it is off. an intensity level which becomes possible [transmitting the quantity of light from which the pel of arbitration differs by supplying different level or the drain electrical potential difference of a value], and is different to a user -- or -- "Gray scale" It can see for having. There are Pulse Density Modulation (PWM) and Pulse Amplitude Modulation (Pulse Amplitude Modulation) in the conventional method of attaining various gray scales. In PWM, the drain electrical potential difference of immobilization is supplied between different time periods determined with pulse width. in Pulse Amplitude Modulation, a different drain electrical potential difference is the same -- time amount (fixed pulse width) supply is carried out. Pulse Amplitude Modulation is high-end TFT LCD. It is suitable for a monitor. By using Pulse Amplitude Modulation, the average polarity of a pel changes with the optical transmissibility of a pel, and gray adjustment is performed. In Pulse Amplitude Modulation, the transmissibility of a pel is controlled by the analog value of the electrical potential difference supplied to the drain line of a direct pel, and, on the other hand, activation of the gate line of a pel is carried out by the digital gate signal.
[0004] In the present LCD manufacture process, the transmissibility of the pel of the range in which homogeneity or prediction is completely possible is not produced to the bias voltage supplied to the drain of a pel. Although the shape of a basic form of a transmissibility curve is known well, the absolute value changes a lot between the displays produced through a production process. Furthermore, human being's vision complicates a situation. because, human being's vision -- a gray scale -- the primary gradation -- contrary -- a logarithm -- it is because it catches-like. this -- the number of gray scales -- a multiplier -- by increasing by "n", it is required for a contrast ratio to increase by n (root2) -- meaning a certain thing, contrast ratio CR is the ratio of the maximum transmissibility to the minimum transmissibility here.

[0005] In manufacture of arbitration, presetting of the different drain electrical-potential-difference value used for Pulse Amplitude Modulation is carried out to the same value to all indicating equipments, or the works calibration of each indicating equipment is carried out separately. The problem in the former approach is the big difference of the display between different indicating equipments, and in order to produce on the level which can be accepted, it is the point that the number of level of a gray scale must be restricted. The latter approach makes the cost of an indicating equipment increase, and consideration to the life of a component, such as making it not take time amount too much to early setting etc., is not given.

[0006]
[Problem(s) to be Solved by the Invention] The object of this invention offers the improved LCD TFT display which has a fixture self-calibration system.

[0007] The object of this invention is TFT LCD which carries out the calibration of the display periodically and realizes the maximum number of gray-scale level in between perfect ONOFU. The self-calibration system of a sake is offered.

[0008]
[Means for Solving the Problem] According to this invention, it is TFT LCD. It has a pel matrix, a different drain electrical potential difference is supplied to the drain line of TFT different here, and a display realizes the number of gray scales set up beforehand. A different drain electrical potential difference is set through a test pel into a calibration. These test pels have the substantially same property as the pel looked at by the user. The property of a test pel is measured first and the control value of the drain electrical potential difference for realizing a different gray scale is extracted from said measurement.

[0009]
[Example] the example of the data processing system which will carry out this invention if drawing 1 is referred to -- being shown -- this system -- a personal computer 10 -- containing -- this -- PC DOS -- or -- It operates under operating systems, such as OS/2, and an application program is performed. For a computer 10, including a microprocessor 12, this is connected to a local bus 14 and a local bus 14 is the bus interface control unit (BIC) 16, the mathematical co-processor 18, and SCSI (small computersystem interface). It connects with an adapter 20. A microprocessor 12 is one of the 80xxx microprocessor families, such as 80386, suitably, and a local bus 14 includes the data, the conventional address, and the conventional control line which suit the architecture of such a processor. An adapter 20 is connected also to the SCSI bus 22, and this bus is connected to the SCSI hard drive (HD) 24 specified as C:drive. A SCSI bus is connectable with other SCSI devices (not shown) again. An adapter 20 is further connected also to NVRAM30 and read-only memory (ROM) 32.

[0010] BIC16 performs the two main functions and one is the function of the memory control unit for accessing main memory 36 and ROM38. Main memory is dynamic random access memory (RAM), and this is constituted by two or more single in-line memory modules (SIMM), and memorizes the program and data which are performed by a microprocessor 12 and the mathematical co-processor 18. Memory 36 memorizes the display program 42 for transmitting data to a display subsystem, and is later mentioned about this. ROM38 memorizes a POST program. The POST program 40 performs POST of a primary test, i.e., a system, when the restart of the computer 10 is carried out by power on or the keyboard reset. The address and a control bus 37 connect BIC16 to memory 36 and ROM38. A data bus 39 connects memory 36 and ROM48 to a data buffer 41, and a data buffer 41 is further connected to data bus 14D of a bus 14. A control line 45 interconnects BIC16 and a data buffer 41.

[0011] Other main functions of BIC16 are the interfaces between the bus 14 by (micro-channel MC) architecture, and an input/output bus 44. A bus 44 is further connected to an input/output control unit (IOC) 46, the graphics control unit 48 and two or more MC connectors, or a slot 50. A control device 48 is further connected to Video RAM (VRAM) 60 and the LCD subsystem 62.

[0012] IOC46 controls the operation of two or more I/O devices, and the floppy disk drive 72 specified as A:drive, a printer 74, and a keyboard 76 are contained in these. Drive 72 contains the floppy disk or diskette 73 in which a control device (not shown) and ejection are possible. IOC46 is connected also to

the mouse connector 78, the serial port connector 80, and the loudspeaker connector 81 again, and these connect various optional equipments to a system.
[0013] When drawing 2 is referred to, the LCD subsystem 62 is TFT LCD64 which has the pel constituted by the matrix of a "j"train x"k" line. It contains. A typical matrix consists of 640 train x480 lines. Gate line 66-k is connected to the gate of all the pels in each line from two or more gate lines 66-1, and a gate signal is supplied to the line of a pel. Drain line 68-j is connected to the drain line of each pel of a different train from two or more drain lines 68-1, and a drain voltage signal is supplied to the train of a pel. The gate line 66 is driven by the line driver 69, and drives the drain line 68 by the train driver 70. as for each pel, a gate signal and a drain voltage signal are supplied simultaneously -- or activation is carried out by connecting the level on a gate line and the drain line 68 to each pel, respectively.
[0014] The line driver 69 operates with a CLK signal and a horizontal scanning (HSCAN) signal as usual, and the latter signal is supplied from timing and a control circuit 82. A CLK signal is supplied to a circuit 82 with a horizontal synchronization (HSYNC) signal and a vertical-synchronization (VSYNC) signal. The two latter signals are supplied with a CLK signal and a data signal also to train timing and a control circuit 84. This data signal is supplied from a control unit 48 and VRAM60, and the digital value showing the gray-scale level displayed on each pel is included in each signal. A circuit 82 and a circuit 84 generate the gate signal and drain signal which synchronize, operate and are promptly supplied to LCD64, and generate the display by data for a user to see by that cause.
[0015] This outputs a series of digital control signals of the "n" bit for a vertical scanning (VSCAN) and a data signal to line 88-j respectively including the RATCHIDO shift register 86 of plurality [driver / 70 / train] from the reception from a circuit 84, and two or more lines 88-1. The number of "n" is the number (2n) of the gray-scale level which can realize on a display technical target and is made into the object. Or it is chosen based on the number of intensity levels, or is determined in advance. A line 88 is connected to demultiplexer (DEMUX) 90-j from two or more demultiplexers (DEMUX) 90-1, respectively, and these outputs are connected to the drain line 68, respectively.
[0016] Two or more 2n The level latch (LL) 94 is connected to the input of the digital-to-analog converter (D/A) 92 of plurality [output / the] respectively. For LL94, it is loaded between calibrations so that it may be mentioned later, and a digital control signal is 2n. The brightness value which defines the drain electrical potential difference of the level from which a phase differs is expressed. These control values are 2n by D/A converter 92. It is changed into the analog drain electrical potential difference of the level from which a phase differs, and these electrical potential differences are transmitted to DEMUX90. Each DEMUX drives one of a voltage level which appears in the output of 92 on the drain line 68, one pel in the train which receives an activation gate signal by that cause is driven, and the intensity level depending on the data signal value supplied to DEMUX in this way is expressed. The value transmitted from the calibration system 96 between calibration processings is loaded to LL94, and this is explained in full detail behind.
[0017] LCD64 has the opaque mask 100 surrounding the above-mentioned pel matrix, and the test pel 98 is arranged from a user behind the mask which cannot be seen. It connects with the calibration system 96 and a test pel operates the photodiode 102 shown in drawing 3 . If drawing 3 is referred to, the test pel 98 will be formed in a visible pel and coincidence, will have the same property as this, and will offer the reliable test for the calibration of an indicating equipment. A photodiode 102 is arranged so that the light in which a pel 98 emits light may be received, and it generates the output voltage which shows the brightness of such a light. A pel 98 receives a gate signal from a gate driver 104, and receives a drain signal from D/A converter 106 between calibrations. A transducer 106 has the same transfer characteristic as a transducer 92, and the analog output value is the same to the digital input value of arbitration. A gate driver 104 is a free running oscillator, and is in agreement with the frequency and duty cycle of a visible pel. Between calibrations, a test pel is driven with the same refresh frequency as the case of a visible pel, and offers the direct correlation with the property of a test pel, and it of a visible pel. Manufacture of a certain display may produce some difference in the property of each pel. Although the activity of a single test pel needs to offer the accuracy of the test which can be accepted, two or more test pels are used into the example of this invention, and acquiring still higher accuracy is also included

by averaging these results.
[0018] The calibration system 96 has digital data processing system, and a microprocessor 108 is connected to RAM110, ROM112, a decoder 126, and a digital-to-analog converter (D/A) 106 for this by the bus 118 including a microprocessor 108. This is selectively performed in a microprocessor 108 by memorizing 114 in a calibration program or a routine, and ROM112 performs a calibration. A calibration is performed at the time of the power on of the beginning of LCD, or when a processor 12 (drawing 1) performs the POST program 40 and passes self-test control to a display system, it is performed. When change of temperature, an atmospheric pressure, etc. affects a display about a display technique, a calibration may be dynamically performed according to such a change of state. Between calibrations, the analog output (DO) of a photodiode 102 is amplified by the amplifier 122, then, is digitized by the analog-digital converter (A/D) 124, is transmitted on a bus 118, and is memorized by the table 116. A table 116 memorizes the digital test value (DV) which generated each analog value DO again.
[0019] The calibration system 96 operates in a test mode and tri-state mode. A system 96 is connected effective in LL94, and the inside of a test mode performs a calibration test first, and then loads a level latch. Then, a system 96 is switched to tri-state mode, it is cut from LL94, and the digital control value memorized by LL94 offers the gray-scale level of the object for operating LCD64. If drawing 4 is referred to and the calibration routine 114 will be performed by the processor 108, step 130 will be measured as a function of a series of test drain electrical-potential-difference values to which the output voltage of a photodiode 102 is supplied by the test pel 98. In such measurement, a table 116 is generated in RAM110 and the value of the test drain electrical potential difference DV corresponding to the photodiode output DO is memorized. The number of the test value acquired during a test or samples is larger than the number of level of the gray value beforehand determined in the display system of arbitration (for example, 100 times). Thereby, gray shading reinforcement is optimized.
[0020] Next, in order to generate the drain electrical potential difference corresponding to the gray-scale level of the "n" phase at step 134, the control value from which it differs for loading to LL94 is chosen. It opts for this selection at step 136, and the mathematical analysis of the test drain volt input to the pel 98 to a photodiode output is performed here. Such analysis is suitably carried out using either two formulas shown below or an equation.
[0021]
X(y+1) =X(y) *root2 (1)
[0022] Here, the value of the range of 1 to "n" and "n of the minimum diode output and y by which the diode output corresponding to the gray-scale level of eye (y) watch in the diode output corresponding to the gray-scale level of eye watch (y+1) in X (y+1) and X (y) and X (1) are detected during a test" are the numbers of gray-scale level.
[0023] n It is shown by n = ln(CR)/(ln 2) (/2), and "CR" is a contrast ratio, "ln" is a standard natural logarithm and "n" is omitted by the integer here.
[0024]
X(y+1)=X(y)*eln CR/n (2)
[0025] Here, e is the bottom of a natural logarithm and all other terms are already definition ending.
[0026] By the activity of a formula 1, a gray-scale step ratio is about 1.4. It is generated and it is considered that this is the minimum ratio about the approaching brightness or gray-scale level which human being can identify. At a formula 2, it is 1.4. A big step ratio is generated, as a result, a display will be discontinuous about brightness more and the difference of contrast can be identified now between the approaching level. If the step level of diode is determined, a table 116 is accessed, and the lookup of the DV value which generates such level will be carried out, and it will memorize in LL94 by making into a digital control value digital value chosen at step 138 next. This transmits a digital control value on a bus 118, and is latched by the latch signal by which this is sent through a line 128 from a decoder 126. In the usual operation after calibration completion, the drain line electrical potential difference of various level is repeatedly supplied to a pel by Pulse Amplitude Modulation as a fixed width-of-face pulse, and generates a different gray scale.

[0027] Although the above-mentioned detailed calibration processing has been described about Monochrome LCD, it will be understood by this contractor by carrying out a calibration similarly to the liquid crystal of red, Green, and blue (RGB) that the above-mentioned processing is applicable also about colorization LCD. Moreover, it will be understood by this contractor that other modification in a detail is also possible, without deviating out of the example of this invention.

[0028]

[Effect of the Invention] As explained above, according to this invention, the calibration of the display is carried out periodically and the self-calibration system of TFT LCD which realizes gray-scale level of the maximum number between perfect ON and off level can be offered.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application] This invention relates to an improvement of the intensity control of LCD which maximizes the number of brightness or gray-scale level by the self-calibration especially about the improvement of a thin film transistor (TFT) liquid crystal display (LCD) system which operates in digital one.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] Generally LCD is formed of the pixel or pel (PEL) in which each contains TFT, and these TFT(s) are combined with the liquid crystal ingredient which transmits light according to the control signal supplied. The transmissibility or the apparent brightness of a pel is the polar function of a liquid crystal ingredient, and this is a function of time amount with which such an electrical potential difference is supplied in connection with the magnitude and the gate signal of a drain electrical potential difference. although the parasitic capacitance which accompanies TFT memorizes DC value temporarily after a control signal is supplied, in order that this may maintain the target transmissibility in a long duration period -- refresh -- or it needs to be re-charged.
[0003] It is difficult to maintain many exact steps about transmissibility about a LCD monitor or a display, perfect ON of a pel, or while it is off. an intensity level which becomes possible [transmitting the quantity of light from which the pel of arbitration differs by supplying different level or the drain electrical potential difference of a value], and is different to a user -- or -- "Gray scale" It can see for having. There are Pulse Density Modulation (PWM) and Pulse Amplitude Modulation (Pulse Amplitude Modulation) in the conventional method of attaining various gray scales. In PWM, the drain electrical potential difference of immobilization is supplied between different time periods determined with pulse width. in Pulse Amplitude Modulation, a different drain electrical potential difference is the same -- time amount (fixed pulse width) supply is carried out. Pulse Amplitude Modulation is high-end TFT LCD. It is suitable for a monitor. By using Pulse Amplitude Modulation, the average polarity of a pel changes with the optical transmissibility of a pel, and gray adjustment is performed. In Pulse Amplitude Modulation, the transmissibility of a pel is controlled by the analog value of the electrical potential difference supplied to the drain line of a direct pel, and, on the other hand, activation of the gate line of a pel is carried out by the digital gate signal.
[0004] In the present LCD manufacture process, the transmissibility of the pel of the range in which homogeneity or prediction is completely possible is not produced to the bias voltage supplied to the drain of a pel. Although the shape of a basic form of a transmissibility curve is known well, the absolute value changes a lot between the displays produced through a production process. Furthermore, human being's vision complicates a situation. because, human being's vision -- a gray scale -- the primary gradation -- contrary -- a logarithm -- it is because it catches-like. this -- the number of gray scales -- a multiplier -- by increasing by "n", it is required for a contrast ratio to increase by n (root2) -- meaning a certain thing, contrast ratio CR is the ratio of the maximum transmissibility to the minimum transmissibility here.
[0005] In manufacture of arbitration, presetting of the different drain electrical-potential-difference value used for Pulse Amplitude Modulation is carried out to the same value to all indicating equipments, or the works calibration of each indicating equipment is carried out separately. The problem in the former approach is the big difference of the display between different indicating equipments, and in order to produce on the level which can be accepted, it is the point that the number of level of a gray scale must be restricted. The latter approach makes the cost of an indicating equipment increase, and consideration to the life of a component, such as making it not take time amount too much to early

setting etc., is not given.
[0006]

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, according to this invention, the calibration of the display is carried out periodically and the self-calibration system of TFT LCD which realizes gray-scale level of the maximum number between perfect ON and off level can be offered.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] The object of this invention offers the improved LCD TFT display which has a fixture self-calibration system.
[0007] The object of this invention is TFT LCD which carries out the calibration of the display periodically and realizes the maximum number of gray-scale level in between perfect ONOFU. The self-calibration system of a sake is offered.

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MEANS

[Means for Solving the Problem] According to this invention, it is TFT LCD. It has a pel matrix, a different drain electrical potential difference is supplied to the drain line of TFT different here, and a display realizes the number of gray scales set up beforehand. A different drain electrical potential difference is set through a test pel into a calibration. These test pels have the substantially same property as the pel looked at by the user. The property of a test pel is measured first and the control value of the drain electrical potential difference for realizing a different gray scale is extracted from said measurement.

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EXAMPLE

[Example] the example of the data processing system which will carry out this invention if drawing 1 is referred to -- being shown -- this system -- a personal computer 10 -- containing -- this -- PC DOS -- or -- It operates under operating systems, such as OS/2, and an application program is performed. For a computer 10, including a microprocessor 12, this is connected to a local bus 14 and a local bus 14 is the bus interface control unit (BIC) 16, the mathematical co-processor 18, and SCSI (small computersystem interface). It connects with an adapter 20. A microprocessor 12 is one of the 80xxx microprocessor families, such as 80386, suitably, and a local bus 14 includes the data, the conventional address, and the conventional control line which suit the architecture of such a processor. An adapter 20 is connected also to the SCSI bus 22, and this bus is connected to the SCSI hard drive (HD) 24 specified as C:drive. A SCSI bus is connectable with other SCSI devices (not shown) again. An adapter 20 is further connected also to NVRAM30 and read-only memory (ROM) 32.
[0010] BIC16 performs the two main functions and one is the function of the memory control unit for accessing main memory 36 and ROM38. Main memory is dynamic random access memory (RAM), and this is constituted by two or more single in-line memory modules (SIMM), and memorizes the program and data which are performed by a microprocessor 12 and the mathematical co-processor 18. Memory 36 memorizes the display program 42 for transmitting data to a display subsystem, and is later mentioned about this. ROM38 memorizes a POST program. The POST program 40 performs POST of a primary test, i.e., a system, when the restart of the computer 10 is carried out by power on or the keyboard reset. The address and a control bus 37 connect BIC16 to memory 36 and ROM38. A data bus 39 connects memory 36 and ROM48 to a data buffer 41, and a data buffer 41 is further connected to data bus 14D of a bus 14. A control line 45 interconnects BIC16 and a data buffer 41.
[0011] Other main functions of BIC16 are the interfaces between the bus 14 by (micro-channel MC) architecture, and an input/output bus 44. A bus 44 is further connected to an input/output control unit (IOC) 46, the graphics control unit 48 and two or more MC connectors, or a slot 50. A control device 48 is further connected to Video RAM (VRAM) 60 and the LCD subsystem 62.
[0012] IOC46 controls the operation of two or more I/O devices, and the floppy disk drive 72 specified as A:drive, a printer 74, and a keyboard 76 are contained in these. Drive 72 contains the floppy disk or diskette 73 in which a control device (not shown) and ejection are possible. IOC46 is connected also to the mouse connector 78, the serial port connector 80, and the loudspeaker connector 81 again, and these connect various optional equipments to a system.
[0013] When drawing 2 is referred to, the LCD subsystem 62 is TFT LCD64 which has the pel constituted by the matrix of a "j"train x"k" line. It contains. A typical matrix consists of 640 train x480 lines. Gate line 66-k is connected to the gate of all the pels in each line from two or more gate lines 66-1, and a gate signal is supplied to the line of a pel. Drain line 68-j is connected to the drain line of each pel of a different train from two or more drain lines 68-1, and a drain voltage signal is supplied to the train of a pel. The gate line 66 is driven by the line driver 69, and drives the drain line 68 by the train driver 70. as for each pel, a gate signal and a drain voltage signal are supplied simultaneously -- or activation is carried out by connecting the level on a gate line and the drain line 68 to each pel, respectively.

[0014] The line driver 69 operates with a CLK signal and a horizontal scanning (HSCAN) signal as usual, and the latter signal is supplied from timing and a control circuit 82. A CLK signal is supplied to a circuit 82 with a horizontal synchronization (HSYNC) signal and a vertical-synchronization (VSYNC) signal. The two latter signals are supplied with a CLK signal and a data signal also to train timing and a control circuit 84. This data signal is supplied from a control unit 48 and VRAM60, and the digital value showing the gray-scale level displayed on each pel is included in each signal. A circuit 82 and a circuit 84 generate the gate signal and drain signal which synchronize, operate and are promptly supplied to LCD64, and generate the display by data for a user to see by that cause.

[0015] This outputs a series of digital control signals of the "n" bit for a vertical scanning (VSCAN) and a data signal to line 88-j respectively including the RATCHIDO shift register 86 of plurality [driver / 70 / train] from the reception from a circuit 84, and two or more lines 88-1. The number of "n" is the number (2n) of the gray-scale level which can realize on a display technical target and is made into the object. Or it is chosen based on the number of intensity levels, or is determined in advance. A line 88 is connected to demultiplexer (DEMUX) 90-j from two or more demultiplexers (DEMUX) 90-1, respectively, and these outputs are connected to the drain line 68, respectively.

[0016] Two or more 2n The level latch (LL) 94 is connected to the input of the digital-to-analog converter (D/A) 92 of plurality [output / the] respectively. For LL94, it is loaded between calibrations so that it may be mentioned later, and a digital control signal is 2n. The brightness value which defines the drain electrical potential difference of the level from which a phase differs is expressed. These control values are 2n by D/A converter 92. It is changed into the analog drain electrical potential difference of the level from which a phase differs, and these electrical potential differences are transmitted to DEMUX90. Each DEMUX drives one of a voltage level which appears in the output of 92 on the drain line 68, one pel in the train which receives an activation gate signal by that cause is driven, and the intensity level depending on the data signal value supplied to DEMUX in this way is expressed. The value transmitted from the calibration system 96 between calibration processings is loaded to LL94, and this is explained in full detail behind.

[0017] LCD64 has the opaque mask 100 surrounding the above-mentioned pel matrix, and the test pel 98 is arranged from a user behind the mask which cannot be seen. It connects with the calibration system 96 and a test pel operates the photodiode 102 shown in drawing 3 . If drawing 3 is referred to, the test pel 98 will be formed in a visible pel and coincidence, will have the same property as this, and will offer the reliable test for the calibration of an indicating equipment. A photodiode 102 is arranged so that the light in which a pel 98 emits light may be received, and it generates the output voltage which shows the brightness of such a light. A pel 98 receives a gate signal from a gate driver 104, and receives a drain signal from D/A converter 106 between calibrations. A transducer 106 has the same transfer characteristic as a transducer 92, and the analog output value is the same to the digital input value of arbitration. A gate driver 104 is a free running oscillator, and is in agreement with the frequency and duty cycle of a visible pel. Between calibrations, a test pel is driven with the same refresh frequency as the case of a visible pel, and offers the direct correlation with the property of a test pel, and it of a visible pel. Manufacture of a certain display may produce some difference in the property of each pel. Although the activity of a single test pel needs to offer the accuracy of the test which can be accepted, two or more test pels are used into the example of this invention, and acquiring still higher accuracy is also included by averaging these results.

[0018] The calibration system 96 has digital data processing system, and a microprocessor 108 is connected to RAM110, ROM112, a decoder 126, and a digital-to-analog converter (D/A) 106 for this by the bus 118 including a microprocessor 108. This is selectively performed in a microprocessor 108 by memorizing 114 in a calibration program or a routine, and ROM112 performs a calibration. A calibration is performed at the time of the power on of the beginning of LCD, or when a processor 12 (drawing 1) performs the POST program 40 and passes self-test control to a display system, it is performed. When change of temperature, an atmospheric pressure, etc. affects a display about a display technique, a calibration may be dynamically performed according to such a change of state. Between calibrations, the analog output (DO) of a photodiode 102 is amplified by the amplifier 122, then, is

digitized by the analog-digital converter (A/D) 124, is transmitted on a bus 118, and is memorized by the table 116. A table 116 memorizes the digital test value (DV) which generated each analog value DO again.
[0019] The calibration system 96 operates in a test mode and tri-state mode. A system 96 is connected effective in LL94, and the inside of a test mode performs a calibration test first, and then loads a level latch. Then, a system 96 is switched to tri-state mode, it is cut from LL94, and the digital control value memorized by LL94 offers the gray-scale level of the object for operating LCD64. If drawing 4 is referred to and the calibration routine 114 will be performed by the processor 108, step 130 will be measured as a function of a series of test drain electrical-potential-difference values to which the output voltage of a photodiode 102 is supplied by the test pel 98. In such measurement, a table 116 is generated in RAM110 and the value of the test drain electrical potential difference DV corresponding to the photodiode output DO is memorized. The number of the test value acquired during a test or samples is larger than the number of level of the gray value beforehand determined in the display system of arbitration (for example, 100 times). Thereby, gray shading reinforcement is optimized.
[0020] Next, in order to generate the drain electrical potential difference corresponding to the gray-scale level of the "n" phase at step 134, the control value from which it differs for loading to LL94 is chosen. It opts for this selection at step 136, and the mathematical analysis of the test drain volt input to the pel 98 to a photodiode output is performed here. Such analysis is suitably carried out using either two formulas shown below or an equation.
[0021]
X(y+1) =X(y) *root2 (1)
[0022] Here, the value of the range of 1 to "n" and "n of the minimum diode output and y by which the diode output corresponding to the gray-scale level of eye (y) watch in the diode output corresponding to the gray-scale level of eye watch (y+1) in X (y+1) and X (y) and X (1) are detected during a test" are the numbers of gray-scale level.
[0023] n It is shown by n = ln(CR)/(ln 2) (/2), and "CR" is a contrast ratio, "ln" is a standard natural logarithm and "n" is omitted by the integer here.
[0024]
X(y+1)=X(y)*eln CR/n (2)
[0025] Here, e is the bottom of a natural logarithm and all other terms are already definition ending.
[0026] By the activity of a formula 1, a gray-scale step ratio is about 1.4. It is generated and it is considered that this is the minimum ratio about the approaching brightness or gray-scale level which human being can identify. At a formula 2, it is 1.4. A big step ratio is generated, as a result, a display will be discontinuous about brightness more and the difference of contrast can be identified now between the approaching level. If the step level of diode is determined, a table 116 is accessed, and the lookup of the DV value which generates such level will be carried out, and it will memorize in LL94 by making into a digital control value digital value chosen at step 138 next. This transmits a digital control value on a bus 118, and is latched by the latch signal by which this is sent through a line 128 from a decoder 126. In the usual operation after calibration completion, the drain line electrical potential difference of various level is repeatedly supplied to a pel by Pulse Amplitude Modulation as a fixed width-of-face pulse, and generates a different gray scale.
[0027] Although the above-mentioned detailed calibration processing has been described about Monochrome LCD, it will be understood by this contractor by carrying out a calibration similarly to the liquid crystal of red, Green, and blue (RGB) that the above-mentioned processing is applicable also about colorization LCD. Moreover, it will be understood by this contractor that other modification in a detail is also possible, without deviating out of the example of this invention.
[0028]

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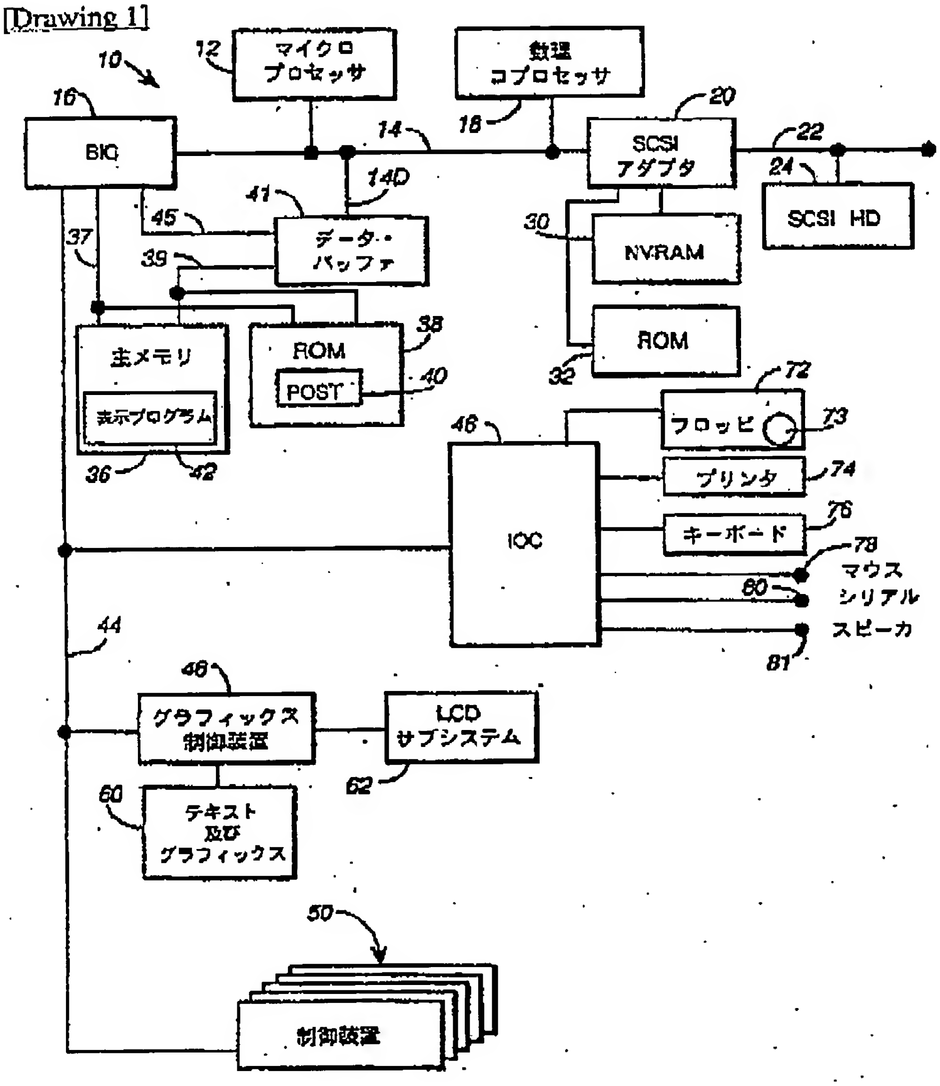
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the data processing system which carries out this invention.
[Drawing 2] It is the block diagram of the LCD subsystem of drawing 1 .
[Drawing 3] It is the block diagram mainly showing the calibration system of the LCD subsystem of drawing 2 .
[Drawing 4] It is outline flow drawing of the calibration processing used by this invention.

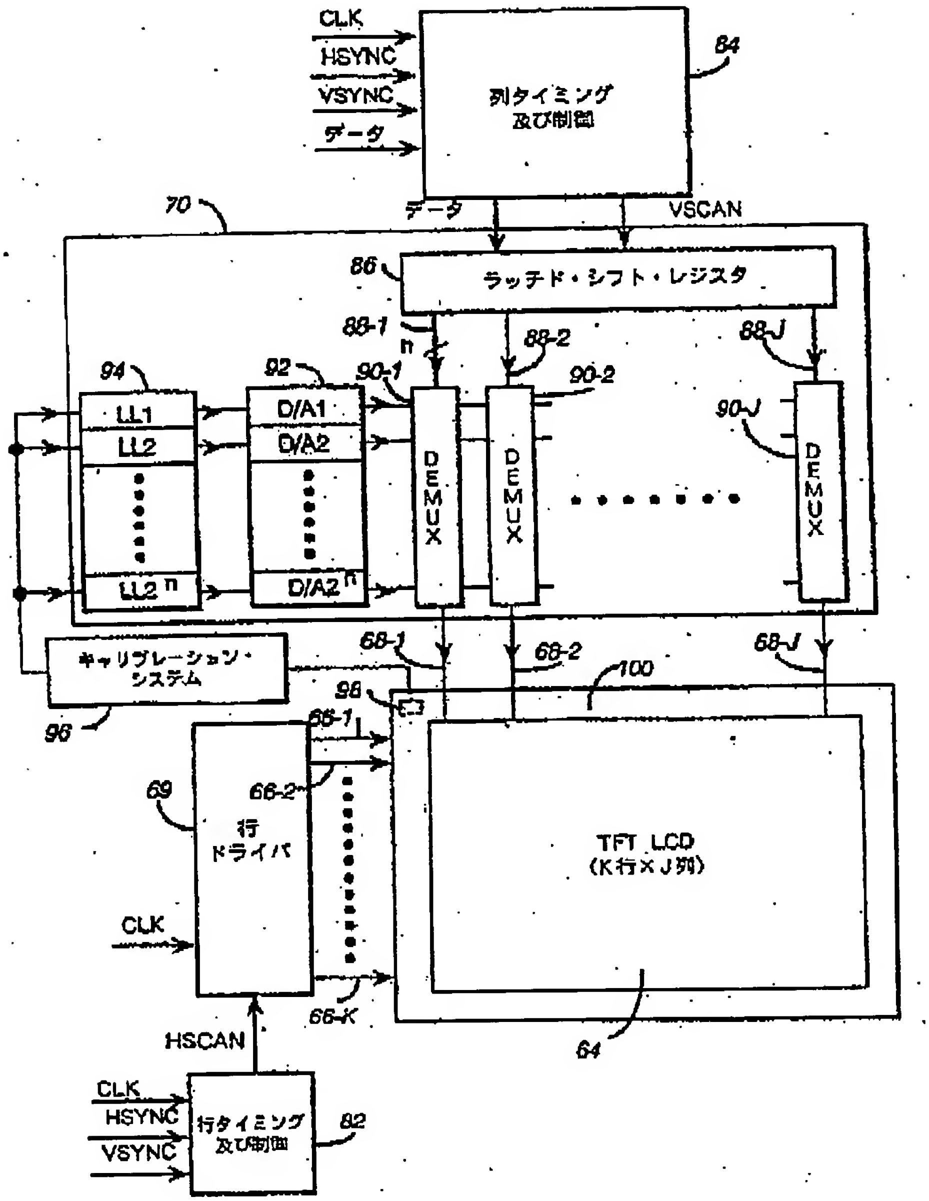
[Translation done.]

DRAWINGS

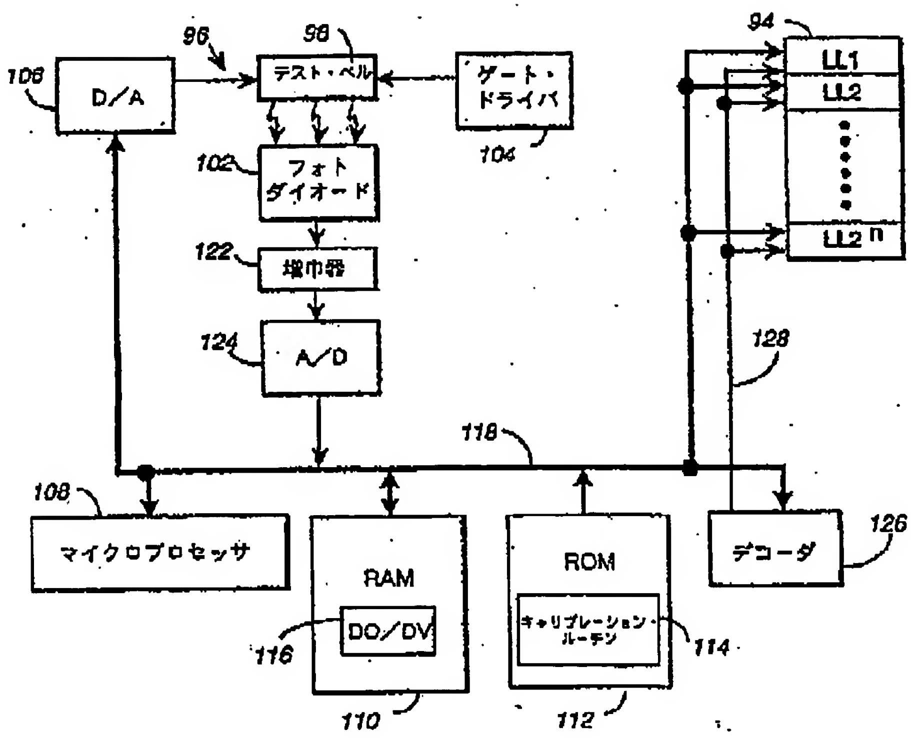
[Drawing 1]



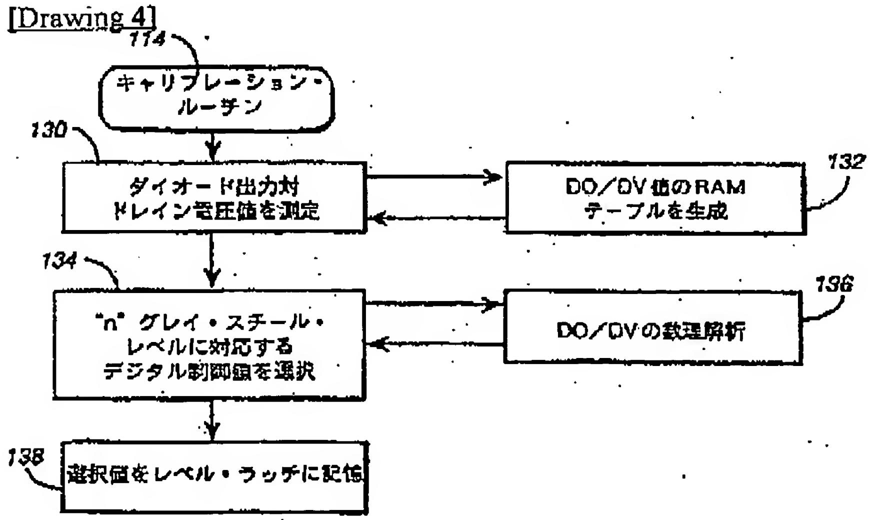
[Drawing 2]


CLK
HSYNC
VSYNC
データ
列タイミング
及び制御
84
70
データ
VSCAN
86
ラッチド・シフト・レジスタ
88-1
n
88-2
88-J
94
92
90-1
90-2
90-J
LL1
LL2
LL2 n
D/A1
D/A2
D/A2 n
DEMUX
DEMUX
DEMUX
68-1
68-2
68-J
キャリブレーション・
システム
100
98
96
66-1
69
66-2
行
ドライバ
TFT LCD
(K行×J列)
CLK
66-K
HSCAN
64
CLK
HSYNC
VSYNC
行タイミング
及び制御
82

[Drawing 3]



[Drawing 4]



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